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(54) **ETCHANT AND ETCHING PROCESS**

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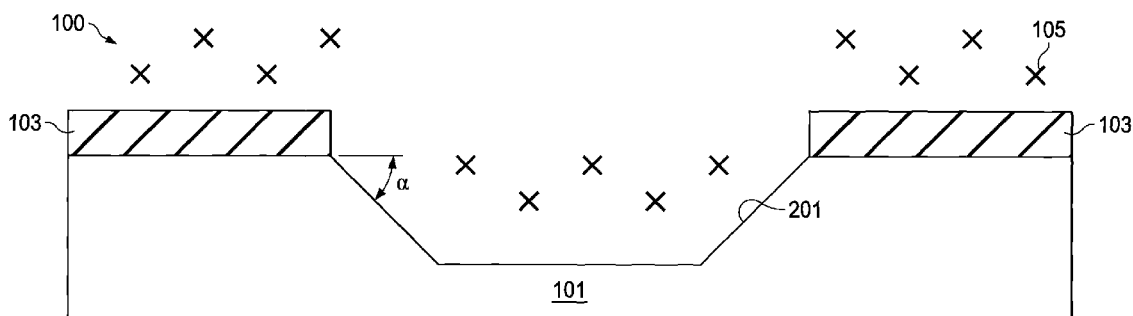
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ABSTRACT

A system and method for manufacturing semiconductor devices is provided. An embodiment comprises using an etchant to remove a portion of a substrate to form an opening with a 45° angle with a major surface of the substrate. The etchant comprises a base, a surfactant, and an oxidant. The oxidant may be hydrogen peroxide.

20 Claims, 3 Drawing Sheets



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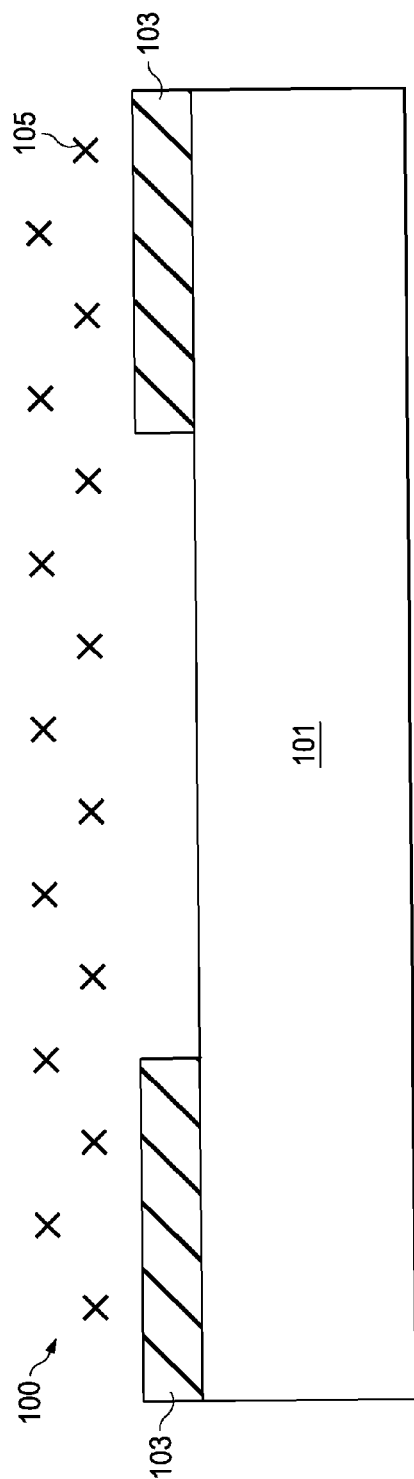


FIG. 1

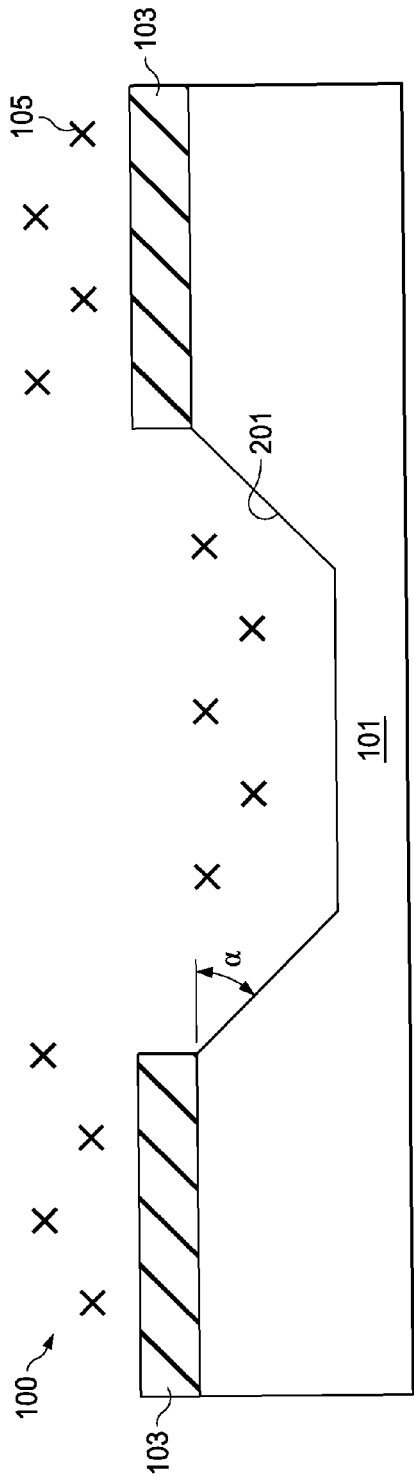


FIG. 2

FIG. 3B

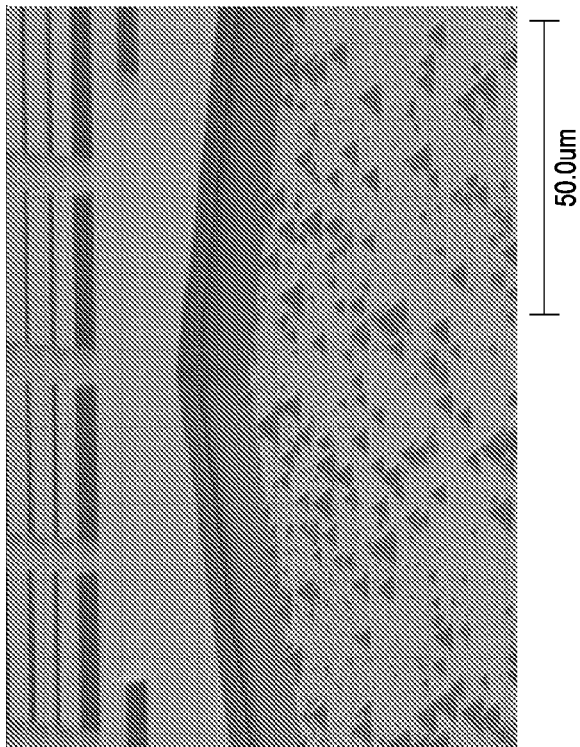
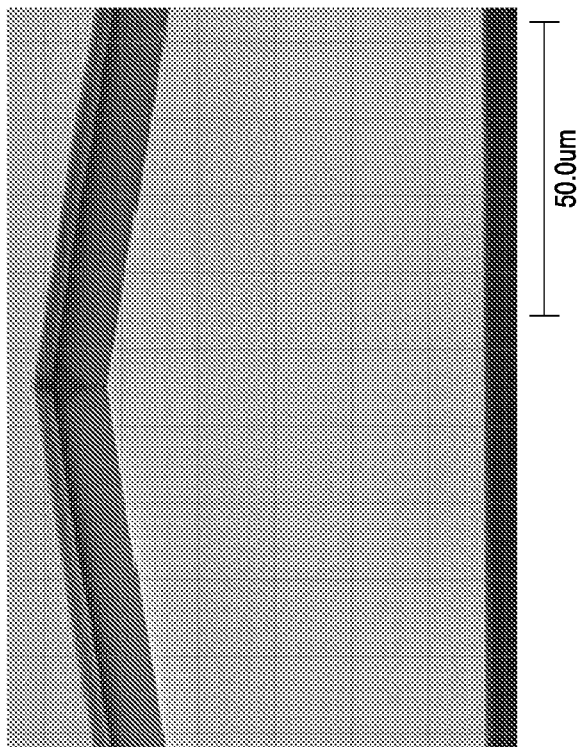
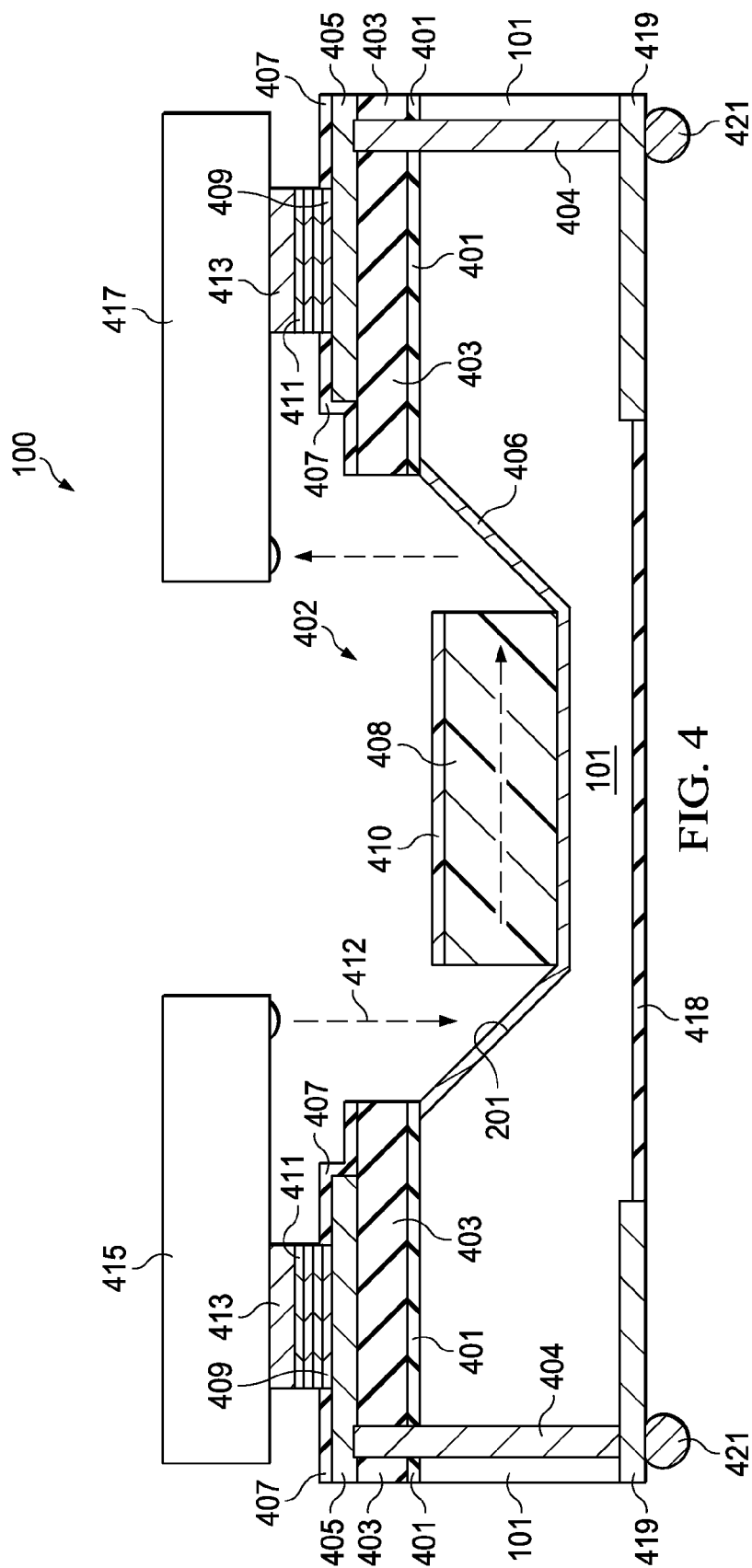


FIG. 3A





ETCHANT AND ETCHING PROCESS

BACKGROUND

Generally, the etching of a substrate material, such as a silicon material, has been utilized in the formation of various structures on the substrate and in the overall manufacturing of semiconductor devices. Such etching generally may utilize a photolithographic masking and etching process. In such a process a photoresist or hardmask is formed on the surface of the substrate and patterned in order to expose a portion of the substrate. Once the photoresist or hard mask has been placed and patterned, the underlying substrate that has been exposed by the hard mask or photoresist is exposed to an etchant by physically applying an etchant or etching solution to the exposed substrate.

Once in contact with the exposed portions of the substrate, the etchant or etching solution will begin to chemically react with the portions of the exposed substrate in which the etchant or etching solution is in contact. This chemical reaction chemically alters the exposed surface of the substrate and removes portions of the substrate from the surface of the substrate, thereby etching into the substrate as the chemical reaction proceeds. Because of the hard mask or photoresist, and the selectivity of the etchant or etching solution to the material of the substrate over the material of the hard mask or photoresist, the removal of material is controlled to occur in those areas of the substrate that are uncovered and exposed by the hard mask or photoresist.

However, each etchant that may be utilized to remove material and form an opening into a material of a substrate, and each etching solution that may be utilized, have various benefits and problems. These include achieving a desired selectivity, obtaining a suitable process controllability, or even limiting the potential drawbacks of the etchant or etching solution.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present embodiments, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIG. 1 illustrates a substrate exposed to an etchant in accordance with an embodiment;

FIG. 2 illustrates a result of the etching process in accordance with an embodiment;

FIGS. 3A-3B illustrate test results between using a described etchant in accordance with an embodiment and using etchants not as described; and

FIG. 4 illustrates a formation additional structures to form a silicon optical bench in accordance with an embodiment.

Corresponding numerals and symbols in the different figures generally refer to corresponding parts unless otherwise indicated. The figures are drawn to clearly illustrate the relevant aspects of the embodiments and are not necessarily drawn to scale.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

The making and using of the present embodiments are discussed in detail below. It should be appreciated, however, that the present disclosure provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are

merely illustrative of specific ways to make and use the disclosed subject matter, and do not limit the scope of the different embodiments.

Embodiments will be described with respect to a specific context, namely a silicon optical bench **100** with a 45 degree reflector. Other embodiments may also be applied, however, to other etching processes.

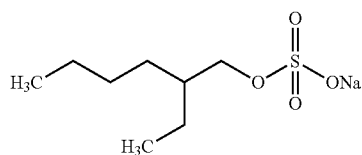
With reference now to FIG. 1, there is shown a cross-sectional, simplified view of a substrate **101** into which an opening **201** (not illustrated in FIG. 1 but illustrated and discussed below with respect to FIG. 2) will be formed. The substrate **101** may comprise a semiconductor material such as silicon, germanium, diamond, or the like, with a crystal orientation of (110) or (100). Alternatively, compound materials such as silicon germanium, silicon carbide, gallium arsenic, indium arsenide, indium phosphide, silicon germanium carbide, gallium arsenic phosphide, gallium indium phosphide, combinations of these, and the like, with other crystal orientations, may also be used. Additionally, the substrate **101** may comprise a silicon-on-insulator (SOI) substrate. Generally, an SOI substrate comprises a layer of a semiconductor material such as epitaxial silicon, germanium, silicon germanium, SOI, silicon germanium on insulator (SGOI), or combinations thereof. The substrate **101** may be doped with a p-type dopant, such as boron, aluminum, gallium, or the like, although the substrate may alternatively be doped with an n-type dopant, as is known in the art.

To form the opening **201** into the substrate **101**, a hardmask **103** may be formed over the substrate **101** and patterned to expose a portion of the substrate **101** into which the opening **201** will be formed. The hardmask **103** may be a masking material such as silicon nitride, and may be formed using a process such as plasma enhanced chemical vapor deposition (PECVD). However, any other suitable hardmask material, such as silicon oxide, and any other process of formation, such as chemical vapor deposition (CVD), may alternatively be utilized. In an embodiment the hardmask **103** may be formed to a thickness of between about 500 Å and about 5000 Å, such as about 1900 Å.

Once formed, the hardmask **103** may be patterned to expose the substrate **101** using, e.g., a photolithographic masking and etching process. In such a process a photoresist (not individually illustrated in FIG. 1) may be placed on the hardmask **103**. The photoresist may comprise a conventional photoresist material, such as a deep ultra-violet (DUV) photoresist, and may be deposited on the surface of the hardmask **103**, for example, by using a spin-on process to place the photoresist. However, any other suitable material or method of forming or placing the photoresist may alternatively be utilized. Once the photoresist has been placed on the hardmask **103**, the photoresist may be exposed to energy, e.g. light, through a patterned reticle in order to induce a reaction in those portions of the photoresist exposed to the energy. The photoresist may then be developed, and portions of the photoresist may be removed, exposing a surface of the hardmask **103**, which may then be etched to remove the exposed portions, thereby patterning the hardmask **103**.

Once the hardmask **103** has been patterned, the substrate **101** exposed by the hardmask **103** may be etched by placing the exposed portions of the substrate **101** into physical contact with an etching solution (illustrated in FIG. 1 by the "X"s labeled **105**). In an embodiment the etching solution **105** may be placed in to contact with the substrate **101** using an wet etching process, whereby the etching solution **105** is placed into contact the substrate **101** by either being sprayed on top of the substrate **101** or else immersing the substrate

However, strong bases such as KOH by themselves do not have the selectivity to control the etching process to etch along a desired crystallographic orientation of, e.g., the first angle α of about 45° . In particular, etching the substrate **101** with an aqueous solution of KOH would result in an angle of 54.7° or even 70° from a major surface of the substrate **101**. As such, in order to modify the selectivity of the strong base to obtain the desired first angle α of about 45° , the surfactant may be added to the etching solution **105**. In an embodiment the surfactant may be a ionic or non-ionic surfactant, and may be a surfactant with a sulfonated base, such as



However, the inclusion of such surfactants within the etching solution **105** also creates additional issues during the process of etching the material of the substrate **101**. In particular, during the etching reaction the surfactant will not

FIG. 2 illustrates a result of using the etching solution **105** described above to etch the substrate **101**. As can be seen, the opening **201** is formed within the substrate **101** and the sidewalls of the opening **201** may be selectively etched to have a 45° angel with a major surface of the substrate **101**. Additionally, with the inclusion of the oxidant within the etching solution **105** the sidewalls and bottom of the opening **201** are formed with a smoother surface due to the lack of micromasking from the oil drops that are formed between the surfactant, the strong base, and the water within the etching solution **105**. Additionally, the inclusion of the

oxidant will also work to inhibit or impede the reverse chemical reaction and help to prevent hillock regrowth during the etching process.

This smoother surface is additionally illustrated in FIGS. 3A-3B, with FIG. 3A illustrating the smooth surface of a material etched utilizing the etching solution 105 described above with respect to FIG. 1 and FIG. 3B illustrating an enlarged surface of a substrate etched with an etching solution 105 of IPA and KOH. As can be seen, the material etched without the inclusion of the oxidant is uneven and rough, with hillocks forming throughout the surface. However, with the use of the etching solution 105 as described, the hillocks are removed along with the rest of the material, resulting in a much smoother and better controlled etching process.

FIG. 4 illustrates a removal of the hardmask 103 and the formation of a waveguide 402 within the opening 201 of the substrate 101. In an embodiment the waveguide 402 may be a polymer waveguide and may be formed along with a reflective material 406, a first passivation layer 401, a second passivation layer 403, through substrate vias (TSVs) 404, a redistribution layer 405, a third passivation layer 407, contact pads 409, underbump metallizations 411, contact bumps 413, an optical generating device 415, and an optical receiving device 417.

The reflective material 406 may be used to increase the amount of light 412 (discussed further below) reflected by the surface of the substrate 101 at the first angle α of about, e.g., 45°. In an embodiment the reflective material 406 may be any material that increases the reflectiveness of the material of the substrate 101, and may be, e.g., a metal such as gold, although any suitable material may alternatively be utilized. The reflective material 406 may be formed using a deposition process such as PVD, CVD, a plating process, combinations of these, or the like. Once formed, the reflective material 406 may be patterned using, e.g., a photolithographic masking and etching process, in order to be located along the sidewalls of the opening 201.

The first passivation layer 401 may be formed on the substrate 101 over the substrate 101. The first passivation layer 401 may be made of one or more suitable dielectric materials such as silicon oxide, silicon nitride, low-k dielectrics such as carbon doped oxides, extremely low-k dielectrics such as porous carbon doped silicon dioxide, combinations of these, or the like. The first passivation layer 401 may be formed through a process such as chemical vapor deposition (CVD), although any suitable process may be utilized, and may have a thickness between about 0.5 μm and about 5 μm , such as about 9.25 KÅ.

The second passivation layer 403 may be formed over the first passivation layer 401. The second passivation layer 403 may be formed from a polymer such as polyimide. Alternatively, the second passivation layer 403 may be formed of a material similar to the material used as the first passivation layer 401, such as silicon oxides, silicon nitrides, low-k dielectrics, extremely low-k dielectrics, combinations of these, and the like. The second passivation layer 403 may be formed to have a thickness between about 2 μm and about 15 μm , such as about 5 μm .

Once the second passivation layer 403 has been formed, the TSVs 404 may be formed to provide a connection through the substrate 101 to an opposite side of the substrate 101. The TSVs 404 may be formed by applying and developing a suitable photoresist, and then etching the substrate 101, the first passivation layer 401 and the second passivation layer 403 to generate TSV openings (filled later as discussed below). The openings for the TSVs 404 at this

stage may be formed so as to extend into the substrate 101 to a depth at least greater than the eventual desired height of the finished silicon optical bench 100. Accordingly, while the depth is dependent upon the overall design of the silicon optical bench 100, the depth may be between about 1 μm and about 700 μm below the surface on the substrate 101, such as a depth of about 50 μm . The openings for the TSVs 404 may be formed to have a diameter of between about 1 μm and about 100 μm , such as about 6 μm .

Once the openings for the TSVs 404 have been formed, the openings for the TSVs 404 may be filled with, e.g., a barrier layer and a conductive material. The barrier layer may comprise a conductive material such as titanium nitride, although other materials, such as tantalum nitride, titanium, a dielectric, or the like may alternatively be utilized. The barrier layer may be formed using a CVD process, such as PECVD. However, other alternative processes, such as sputtering or metal organic chemical vapor deposition (MOCVD), may alternatively be used. The barrier layer may be formed so as to contour to the underlying shape of the opening for the TSVs 404.

The conductive material may comprise copper, although other suitable materials such as aluminum, alloys, doped polysilicon, combinations thereof, and the like, may alternatively be utilized. The conductive material may be formed by depositing a seed layer and then electroplating copper onto the seed layer, filling and overfilling the openings for the TSVs 404. Once the openings for the TSVs 404 have been filled, excess barrier layer and excess conductive material outside of the openings for the TSVs 404 may be removed through a grinding process such as chemical mechanical polishing (CMP), although any suitable removal process may be used.

Once the conductive material is within the openings for the TSVs 404, a thinning of the second side of the substrate 101 may be performed in order to expose the openings for the TSVs 404 and form the TSVs 404 from the conductive material that extends through the substrate 101. In an embodiment, the thinning of the second side of the substrate 101 may leave the TSVs 404. The thinning of the second side of the substrate 101 may be performed by a planarization process such as CMP or etching.

However, as one of ordinary skill in the art will recognize, the above described process for forming the TSVs 404 is merely one method of forming the TSVs 404, and other methods are also fully intended to be included within the scope of the embodiments. For example, forming the openings for the TSVs 404, filling the openings for the TSVs 404 with a dielectric material, thinning the second side of the substrate 101 to expose the dielectric material, removing the dielectric material, and filling the openings for the TSVs 404 with a conductor may also be used. This and all other suitable methods for forming the TSVs 404 into the substrate 101 are fully intended to be included within the scope of the embodiments.

Alternatively, the TSVs 404 may be formed as each of the layers over the substrate 101 are individually formed. For example, the TSVs 404 may be formed partially concurrently with the first passivation layer 401 and the second passivation layer 403. For example, a portion of the openings for the TSVs 404 may be formed and filled within the substrate 101 prior to the formation of the first passivation layer 401, and subsequent layers of the openings for the TSVs 404 may be formed and filled as each of the first passivation layer 401 and the second passivation layer 403 are individually formed. Any of these processes, and any

other suitable process by which the TSVs **404** may be formed, are fully intended to be included within the scope of the embodiments.

After the TSVs **404** have been formed, the first RDL layer **405** may be formed to extend along the second passivation layer **403**. The first RDL layer **405** may be utilized as a redistribution layer to allow the contact pads **409** that are electrically connected to the TSVs **404** to be placed in any desired location on the substrate **101**, instead of limiting the location of the contact pads **409** to the regions directly over the TSVs **404**. In an embodiment the first RDL layer **405** may be formed by initially forming a seed layer (not shown) of a titanium copper alloy through a suitable formation process such as CVD or sputtering. A photoresist (not shown) may then be formed to cover the seed layer, and the photoresist may then be patterned to expose those portions of the seed layer that are located where the first RDL layer **405** is desired to be located.

Once the photoresist has been formed and patterned, a conductive material, such as copper, may be formed on the seed layer through a deposition process such as plating. The conductive material may be formed to have a thickness of between about 1 μm and about 10 μm , such as about 5 μm , and a width along the substrate **101** of between about 5 μm and about 300 μm , such as about 15 μm . However, while the material and methods discussed are suitable to form the conductive material, these materials are merely exemplary. Any other suitable materials, such as AlCu or Au, and any other suitable processes of formation, such as CVD or PVD, may alternatively be used to form the first RDL layer **405**.

Once the conductive material has been formed, the photoresist may be removed through a suitable removal process such as ashing. Additionally, after the removal of the photoresist, those portions of the seed layer that were covered by the photoresist may be removed through, for example, a suitable etch process using the conductive material as a mask.

After the first RDL layer **405** has been formed, the third passivation layer **407** may be formed to cover and protect the first RDL layer **405**. The third passivation layer **407**, similar to the second passivation layer **403**, may be formed from a polymer such as polyimide, or may alternatively be formed of a similar material as the first passivation layer **401** (e.g., silicon oxides, silicon nitrides, low-k dielectrics, extremely low-k dielectrics, combinations of these, and the like). The third passivation layer **407** may be formed to have a thickness of between about 2 μm and about 15 μm , such as about 5 μm .

After the third passivation layer **407** has been formed, a RDL opening may be made through the third passivation layer **407** by removing portions of the third passivation layer **407** to expose at least a portion of the underlying first RDL layer **405**. The RDL opening allows for contact between the UBM **411** and the first RDL layer **405**. The RDL opening may be formed using a suitable photolithographic mask and etching process, although any suitable process to expose portions of the first RDL layer **405** may alternatively be used.

The contact pad **409** may optionally be formed over and in electrical contact with the first RDL layer **405**. The contact pad **409** may comprise aluminum, but other materials, such as copper, may alternatively be used. The contact pad **409** may be formed using a deposition process, such as sputtering, to form a layer of material (not shown) and portions of the layer of material may then be removed through a suitable process (such as photolithographic masking and etching) to form the contact pad **409**. However, any

other suitable process may be utilized to form the contact pad **409**. The contact pad **409** may be formed to have a thickness of between about 0.5 μm and about 4 μm , such as about 1.45 μm .

Once the contact pad **409** has been formed, the UBM **411** may be formed in electrical contact with the contact pad **409**. In an embodiment the UBM **411** may comprise three layers of conductive materials, such as a layer of titanium, a layer of copper, and a layer of nickel. However, one of ordinary skill in the art will recognize that there are many suitable arrangements of materials and layers, such as an arrangement of chrome/chrome-copper alloy/copper/gold, an arrangement of titanium/titanium tungsten/copper, or an arrangement of copper/nickel/gold, that are suitable for the formation of the UBM **411**. Any suitable materials or layers of material that may be used for the UBM **411** are fully intended to be included within the scope of the current application.

The UBM **411** may be created by forming each layer over the third passivation layer **407** and along the interior of the RDL opening through the third passivation layer **407** to the contact pad **409**. The forming of each layer may be performed using a plating process, such as electrochemical plating, although other processes of formation, such as sputtering, evaporation, PECVD process, may alternatively be used depending upon the desired materials. The UBM **411** may be formed to have a thickness of between about 0.7 μm and about 10 μm , such as about 5 μm . Once the desired layers have been formed, portions of the layers may then be removed through a suitable photolithographic masking and etching process to remove the undesired material and to leave the UBM **411** in a desired shape, such as a circular, octagonal, square, or rectangular shape, although any desired shape may alternatively be formed.

The contact bump **413** may comprise a material such as tin, or other suitable materials, such as silver, lead-free tin, copper, or gold. In an embodiment in which the contact bump **413** is a tin solder bump, the contact bump **413** may be formed by initially forming a layer of tin through such commonly used methods such as evaporation, electroplating, printing, solder transfer, ball placement, etc, to a thickness of, e.g., about 100 μm . Once a layer of tin has been formed on the structure, a reflow may be performed in order to shape the material into the desired bump shape.

On a second side of the substrate **101** opposite the first side of the substrate **101** over which the first passivation layer **401** has been formed, a fourth passivation layer **418**, second contact pads **419**, and second contact bumps **421** may be formed. The fourth passivation layer **418**, similar to the second passivation layer **403**, may be formed from a polymer such as polyimide, or may alternatively be formed of a similar material as the first passivation layer **401** (e.g., silicon oxides, silicon nitrides, low-k dielectrics, extremely low-k dielectrics, combinations of these, and the like). The fourth passivation layer **418** may be formed to have a thickness of between about 2 μm and about 15 μm , such as about 5 μm .

The second contact pads **419** may be formed over and in electrical contact with the TSVs **404**. The second contact pads **419** may comprise aluminum, but other materials, such as copper, may alternatively be used. The second contact pads **419** may be formed using a deposition process, such as sputtering, to form a layer of material (not shown) and portions of the layer of material may then be removed through a suitable process (such as photolithographic masking and etching or chemical mechanical polishing) to form the second contact pads **419**. However, any other suitable

process may be utilized to form the second contact pads **419**. The second contact pads **419** may be formed to have a thickness of between about 0.5 μm and about 4 μm , such as about 1.45 μm .

The second contact bumps **421** may comprise a material such as tin, or other suitable materials, such as silver, lead-free tin, or copper. In an embodiment in which the second contact bumps **421** is a tin solder bump, the second contact bumps **421** may be formed by initially forming a layer of tin through such commonly used methods such as evaporation, electroplating, printing, solder transfer, ball placement, etc., to a thickness of, e.g., about 100 μm . Once a layer of tin has been formed on the structure, a reflow may be performed in order to shape the material into the desired bump shape.

Returning to the first side of the substrate **101**, a waveguide **402** may be formed within the opening **201** in order to accept and channel the light **412** to its desired destination (e.g., between an optical generating device **415** and an optical receiving device **417**, both of which are described further below). The waveguide **402** may be any type of waveguide, such as a planar waveguide or a channel waveguide, and may comprise two different materials, a core material **408** and a cladding material **410**, in which the core material **408** has a refractive index higher than the cladding material **410**.

In an embodiment the core material **408** and the cladding material **410** comprise a combination of polymer materials, such as poly(methylmethacrylate) (PMMA), polystyrene (PS), polycarbonate, polyurethane, benzocyclobutane, perfluorovinyl ether cyclopolymer, tetrafluoroethylene, perfluorovinyl ether copolymer, silicone, fluorinated poly(arylene ether sulfide), poly(pentafluoro styrene), fluorinated dendrimers, fluorinated hyperbranched polymers, or the like. Alternatively, the core material **408** and the cladding material **410** may comprise deuterated and halogenated polyacrylates, fluorinated polyimides, perfluorocyclobutyl aryl ether polymers, nonlinear optical polymers, or the like. In yet another embodiment, the core material **408** and the cladding material **410** may comprise silicon or silicon dioxide, to utilize the index of refraction between the materials to confine and constrain the path of the light **412** through the waveguide **402**.

The core material **408** and the cladding material **410** of the waveguide **402** may be formed, e.g., by initially placing each layer or combination of layers onto the substrate **101** using a process such as spin coating, doctor blading, extrusion, lamination, or the like. Once the individual layers are in place, the individual layers may be patterned using, e.g., photolithographic masking and etching techniques to individually or collectively pattern the individual layers to form the desired shape of the waveguide **402**.

Additionally, the waveguide **402** may optionally comprise one or more structures that aid in the transmittal and or conditioning of the light **412**. As examples only, beam splitters, filters, or reflectors (not individually illustrated in FIG. 4) may optionally be included within the waveguide **402** as desired in order to better control and direct the received light **412**. These and all such structures that may be utilized either within or with the waveguide **402** are fully intended to be included within the scope of the embodiments.

An optical generating device **415** may be connected to a first one of the contact bumps **413** in order to convert an electrical signal to an electromagnetic signal such as light **412** that will be constrained by the waveguide **402**. In an embodiment the optical generating device **415** may be a

laser diode, although any other suitable device that can translate an electrical signal to an electromagnetic signal may alternatively be utilized. In an embodiment the optical generating device **415** may be electrically and physically connected to the silicon optical bench **100** by placing the optical generating device **415** in physical connection with the contact bumps **413** and then performing a reflow process to reflow the contact bump **413** and connect the optical generating device **415** to the contact bump **413**.

However, as one of ordinary skill will recognize, the use of a separate optical generating device **415** and its connection with the contact bump **413** is merely one embodiment, and is intended to be illustrative and not limiting. Rather, any suitable type of optical generating device **415** formed and connected to the silicon optical bench **100** in any fashion, may be utilized. For example, the optical generating device **415** may alternatively be a InP group semiconductor laser that is grown using methods such as metal organic vapor deposition onto the substrate **101** without the use of the contact bumps **413**. These and any other suitable type optical generating device **415** that may be utilized to transform an electrical signal to an electromagnetic signal, or to merely direct an optical signal to the waveguide **402**, may alternatively be used, and all such alternatives are fully intended to be included within the scope of the embodiments.

An optical receiving device **417** may be connected to another one of the contact bumps **413** in order to receive the light **412** from the waveguide **402** and transform the received light **412** back into an electrical signal. In an embodiment the optical receiving device **417** may be, e.g., a photodiode used to convert the light **412** to an electrical signal, although any suitable device may alternatively be utilized.

In an embodiment the optical receiving device **417** may be connected to the silicon optical bench **100** using, e.g., another one of the contact bumps **413**. In an embodiment the optical receiving device **417** may be connected by placing the optical receiving device **417** into contact with the contact bump **413** and performing a reflow process to physically and electrically connect the optical receiving device **417** to the contact bump **413**.

However, as one of ordinary skill will recognize, the use of a separate optical receiving device **417** and its connection with the contact bump **413** is merely one embodiment, and is intended to be illustrative and not limiting. Rather, any suitable type of optical receiving device **417** formed and connected to the silicon optical bench **100** in any fashion, may be utilized. For example, the optical receiving device **417** may alternatively be a photodiode grown epitaxially onto the substrate **101** without the use of the contact bumps **413**. These and any other suitable type optical receiving devices **417** that may be utilized to transform an electromagnetic signal to an electrical signal may alternatively be used, and all such alternatives are fully intended to be included within the scope of the embodiments.

During operation, the optical generating device **415** will receive an electrical signal through, e.g., the TSV **404** and convert the electrical signal into light (labeled in FIG. 4 by arrows **412**). The light **412** will travel towards the substrate **101** and be reflected by the reflecting material **406** towards the waveguide **402**, which will guide the light **412** to a desired destination. Once it reaches the destination, the light **412** will exit the waveguide **402**, reflect off the reflecting material **406** and reach the optical receiving device **417**, which will convert the light **412** from an optical signal back to an electrical signal.

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Additionally, while only the optical generating device 415, the waveguide 402, and the optical receiving device 417 are illustrated in FIG. 4, any number of other suitable devices may also be manufactured on the substrate 101 in order to manufacture the silicon optical bench 100. For example, other microwave or optical components may be included in order to transmit and/or process the various electrical and optical signals that will be utilized by the silicon optical bench 100 in order to achieve its desired function. These and all such structures are fully intended to be included within the scope of the embodiments.

In accordance with an embodiment, a method for manufacturing a device comprising masking a substrate with a patterned mask and exposing the substrate through the patterned mask to an etchant is provided. The etchant comprises a base, a surfactant, and an oxidant.

In accordance with another embodiment, a semiconductor material etchant comprising a base, a surfactant, and an oxidant is provided.

In accordance with yet another embodiment, a method of etching a substrate comprising applying an etchant to a substrate, the etchant comprising a base, a surfactant, and an oxidant, is provided. A portion of the substrate is oxidized to change the substrate from hydrophobic to hydrophilic, and an opening is formed in the substrate with the etchant.

Although the present embodiments and their advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the disclosure as defined by the appended claims. For example, many different chemicals may be used with or in place of the chemicals specifically described herein. Additionally, the etching solution and process may be used in the manufacture of different structures than a silicon optical bench, such as microelectromechanical (MEMS) devices.

Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present disclosure. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

What is claimed is:

1. A method for manufacturing a device, the method comprising:

masking a substrate with a patterned mask, wherein the substrate is a waveguide substrate and wherein the masking the substrate with the patterned mask comprises:

blanket applying a first material; and

removing a portion of the first material through a patterned photosensitive material to form the patterned mask;

exposing the substrate through the patterned mask to an etchant, wherein the etchant removes a semiconductor portion of the substrate to form an opening, a first planar surface intersecting the opening, and a second planar surface intersecting the opening on an opposite side of the opening from the first planar surface, the etchant comprising:

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a strong base;
a surfactant; and
an oxidant; and

forming a reflective material over and in physical contact with each surface within the opening, the reflective material extending from the first planar surface to the second planar surface.

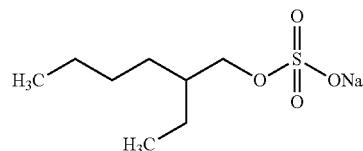
2. The method of claim 1, wherein the base is potassium hydroxide.

3. The method of claim 2, wherein the oxidant is H_2O_2 .

4. The method of claim 2, wherein the oxidant is ozone.

5. The method of claim 2, wherein the oxidant is $KMnO_4$.

6. The method of claim 3, wherein the surfactant has the following structure:



7. The method of claim 3, wherein the surfactant is alkyl based.

8. A method of etching a substrate, the method comprising:

applying an etchant to a first section of an optical bench exposed through a hard mask, the etchant comprising a strong base, a surfactant, and an oxidant;

oxidizing a first portion of the optical bench to change the first portion from hydrophobic to hydrophilic, wherein a second portion of the optical bench remains hydrophobic at the same time as the first portion is hydrophilic, the first portion and the second portion both being laterally removed in a direction parallel with a major surface of the optical bench from sidewalls of the hard mask; and

forming an opening in the optical bench with the etchant.

9. The method of claim 8, wherein the oxidant is H_2O_2 .

10. The method of claim 8, wherein the opening has a 45° angle with a major surface of the optical bench.

11. The method of claim 8, wherein the base comprises KOH and the oxidant comprises one of H_2O_2 , O_3 , or $KMnO_4$.

12. The method of claim 8, further comprising forming a laser diode, a photodiode, and a waveguide on the optical bench.

13. A method of manufacturing a semiconductor device, the method comprising:

preparing an etchant to be applied, wherein the preparing the etchant further comprises:

providing a solvent;

adding a strong base to the solvent;

adding a surfactant to the solvent, wherein the adding the surfactant modifies the selectivity of the etchant to etch along a crystallographic orientation to an angle of 45° ; and

adding an oxidizer to the solvent;

applying the etchant to a semiconductor substrate, wherein the semiconductor substrate is a waveguide substrate and wherein the applying the etchant removes semiconductor material from the semiconductor substrate through a patterned mask located on the semiconductor substrate to form an opening within the semiconductor substrate, wherein after the forming the

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opening the opening has a first sidewall that extends from a planar bottom surface of the opening to a first planar top surface of the semiconductor substrate and has a second sidewall that extends from the planar bottom surface of the opening to a second planar top surface of the semiconductor substrate, wherein the second planar top surface is different from the first planar top surface and wherein the planar bottom surface is planar from the first sidewall to the second sidewall; and

applying a reflective material to each surface within the opening.

14. The method of claim **13**, wherein the applying the etchant to the semiconductor substrate etches an opening into the semiconductor substrate, the opening having a 45° angle with a major surface of the semiconductor substrate.

15. The method of claim **13**, wherein the applying the etchant to the semiconductor substrate etches along a crystallographic orientation of the semiconductor substrate.

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16. The method of claim **13**, wherein after the applying the etchant to the semiconductor substrate the oxidizer oxidizes a surface of the semiconductor substrate to repel by-products of chemical reactions that occur between the etchants and the semiconductor substrate.

17. The method of claim **13**, wherein the strong base is potassium hydroxide.

18. The method of claim **17**, wherein the surfactant is a sulfonated base.

19. The method of claim **18**, wherein the oxidizer is hydrogen peroxide.

20. The method of claim **13**, further comprising forming a waveguide on the semiconductor substrate after the applying the etchant to the semiconductor substrate.

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